St. Joseph's Institute of Technology

St. Joseph's Group of Institutions

OMR, Chennai – 119

Department of Electronics and Communication Engineering

(Accredited by NBA)

FACULTY DETAILS

Staff Name	Dr.J.Jeba Johannah
Designation	Associate Professor
Date of Birth	16-01-1972
Educational Qualification	Ph.D
Area of Interest	Low Power VLSI
Years of Experience	17 years
Area of Research	Low Power VLSI
No. of Students Project Guided	25
Publications Details	• **Jeba Johannah . J , Reeba Korah, Maria Kalavathy.G, "New efficient designs for deep submicron NOR gate on the transistor level", ICRTET, April 2016.** • **Jeba Johannah . J , Reeba Korah, Maria Kalavathy.G and Sivanandhan, "**Standby and dynamic power minimization using enhanced hybrid power gating structure for deep-submicron CMOS VLSI", Microelectronics Journal, Volume 62 Issue C, April 2017, pp. 137-145 • **Jeba Johannah . J , Reeba Korah, Maria Kalavathy.G "**Low-Power Deep-Submicron CMOS Adder Using Optimized Delay Universal Gates", Advances in Automation, Signal Processing, Instrumentation, and Control, Springer book,
FDP & Workshop Attended Details	• FDP on "Testing of VLSI ", KCG College of Engineering, Karapakkam • FDP on "Physical Design of Analog and Digital Circuits using CADENCE Design suite", SRM College of Engineering, Katankulathur

	• FDP on " VLSI Chip Design and Testing using Mentor Graphics", Vellore Institute of Technology, Vellore • FDP on SCILAB, spoken tutorial, IIT Bombay • FDP on "Recent trends in Computational Intelligencefor Healthcare monitoring system", Banari Amman Institute of Technology, Sathyamangalam • FDP on "VLSI physical design using Cadence Innovus Tool", St.Joseph's College of Engineering • FDP on "EC8791- Embedded and real time systems", Saveetha Engineering College, Chennai • FDP on "Machine Learning", Saveetha Engineering College, Chennai • FDP on "ASIC Design Verification using System Verilog", Sandeepam School of Embedded System, Bangalore • FDP on "System Design through Verilog", NPTEL • FDP on "IOT and Cloud Interface", St.Joseph's Institute of Technology • FDP on "Embedded Systems", NPTEL