St. Joseph's Institute of Technology

St. Joseph's Group of Institutions

OMR, Chennai – 119

Department of Electronics and Communication Engineering

(Accredited by NBA)

FACULTY DETAILS

Staff Name:	Dr.J.Jeba Johannah
Designation:	Associate Professor
Date of Birth:	16-01-1972
Educational Qualification:	Ph.D
Area of Interest:	Low Power VLSI
Years of Experience:	14 years
Area of Research:	Low Power VLSI
No. of Students Project Guided	15
Publications Details:	• **Jeba Johannah . J , Reeba Korah, Maria Kalavathy.G, "New efficient designs for deep submicron NOR gate on the transistor level", ICRTET, April 2016.** • **Jeba Johannah . J , Reeba Korah, Maria Kalavathy.G and Sivanandhan, "**Standby and dynamic power minimization using enhanced hybrid power gating structure for deep-submicron CMOS VLSI", Microelectronics Journal, Volume 62 Issue C, April 2017, pp. 137-145
FDP & Workshop Attended Details:	• FDP on "Testing of VLSI ", KCG College of Engineering, Karapakkam • FDP on "Physical Design of Analog and Digital Circuits using CADENCE Design suite", SRM College of Engineering, Katankulathur • FDP on " VLSI Chip Design and Testing using Mentor Graphics", Vellore Institute of Technology, Vellore • FDP on SCILAB, spoken tutorial, IIT Bombay

	• FDP on "EC8791- Embedded and real time systems", Saveetha Engineering College, Chennai
Professional Membership:	Linkedin