St. Joseph's Institute of Technology
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OMR, Chennai – 119

Department of Electronics and Communication Engineering
(Accredited by NBA)

FACULTY DETAILS

Staff Name:	Dr. BHUVANA B P
Designation:	Assistant Professor
Date of Birth:	13.04.1990
Educational Qualification:	BE., ME., Ph.D
Area of Interest:	VLSI DESIGN
Years of Experience:	3 Years and 6 months
Area of Research:	Low Power VLSI Design
No. of Students Project Guided	NA
Publications Details:	**International Journals:** 1. Bhuvana, B. P, V S Kanchana Bhaaskaran. "**Design of FinFET-based Energy Efficient Pass-Transistor Adiabatic Logic for Ultra-Low Power Applications**", Microelectronics Journal, Vol. 92, 2019, pp.104601. **(SCI Indexed) (Impact Factor – 1.405)** 2. Bhuvana, B. P, V S Kanchana Bhaaskaran. "**Design and Analysis of IPAL for Ultra Low Power CRC Architecture for Applications in IoT based Systems**", AEU-International Journal of Electronics and Communications, Vol. 108, 2019, pp.127-40. **(SCI Indexed) (Impact Factor – 2.924)** 3. Bhuvana B P, Kanchana Bhaaskaran V S, "**Analysis of FinFET based Adiabatic circuits for the design of Arithmetic Structures**", Journal of Circuits, Systems and Computers, Vol. 29, No. 1, 2020, pp.2050016. **(SCI Indexed)** (**Impact Factor – 1.363**). 4. Bhuvana B P, Manohar B R, Kanchana Bhaaskaran V S, "**Adiabatic Logic Circuits Using FinFETs and CMOS – A Review**" International Journal of Engineering and Technology, Vol 8 No 2 Apr-May 2016, p-ISSN : 2319-8613. **(SNIP -0.81)** 5. Srinivasa Raghavan B., Bhuvana B.P. and Kanchana

	Bhaaskaran V. S., "**Low Power 64-bit Carry Select Adder using modified EXNOR Block**", ARPN Journal of Engineering and Applied Sciences, Vol. 10, No. 22, Dec 2015, ISSN 1819-6608. **(SNIP -0.473)** 6. Bhuvana, BP. "Reducing Mismatches in the Analog Signal by Using Levenberg-Marquardt Back Propagation Algorithm." World Applied Sciences Journal, Vol.29, No.10, 2014, pp.1320-1326. 7. Bhuvana, B. P. "Comparison of Simple Clustering by Self-Organizing Maps Using Neural Network Clustering Tool." World Applied Sciences Journal, Vol. 29, No. 10, 2014, pp. 1261-1266. 8. Bhuvana, B. P. "Segmentation of Brain MRI Images by Using Modified Robust Fuzzy c Means Algorithm." World Applied Sciences Journal, Vol. 29, No. 10, 2014, pp. 1327-1332. **International Conferences:** 1. Bhuvana B P, and Kanchana Bhaaskaran V S, "**Design of reversible adders using a novel reversible BKG gate**", Green Engineering and Technologies (IC-GET), 2016 Online Inter Conf on. IEEE, 2016, pp. 1-6. 2. Bhuvana B P, Manohar B R and Kanchana Bhaaskaran V S, "**Standard Cell Characterization for Reversible Logic**", Micro-Electronics and Telecommunication Engineering (ICMETE), 2016 International Conference on. IEEE, 2016, pp. 534-538. 3. Bhuvana, B. P., and VS Kanchana Bhaaskaran. "**Quantum Cost Optimization of Reversible Adder/Subtractor Using a Novel Reversible Gate**", In Innovations in Electronics and Communication Engineering, Springer Lecture Notes in Networks and Systems, Singapore, 2018, pp. 111-118. 4. Bhuvana, B. P., and VS Kanchana Bhaaskaran. "**A novel adiabatic logic for low power VLSI circuit design and power optimization using FinFET**", In VLSI Design: Circuits, Systems and Applications, Springer Lecture Notes in Electrical Engineering, Singapore, 2018, pp. 117-126. 5. Bhuvana B P and Kanchana Bhaaskaran V S, "**Performance Analysis of 2N-N-2P Adiabatic Logic Circuits for Low Power Applications using FinFET**" Elsevier Procedia Computer Science, 115, 2017, pp. 166-173. 6. Bhuvana, B. P., and VS Kanchana Bhaaskaran, "**Positive feedback symmetric adiabatic logic against differential power attack.**" 2018 31st International Conference on VLSI Design and 2018 17th International Conference on Embedded Systems

	(VLSID). IEEE, 2018, pp. 149-154. 7. Jayashree K G, Lois Priscilla S, Bhuvana B P, Kanchana Bhaaskaran V S, "**Design and Analysis of FinFET based CSCPAL Low Power Adder**", In 2019 IEEE International Symposium on Smart Electronic Systems (iSES), pp. 139-144. IEEE, 2019 8. B P Bhuvana ; V S Kanchana Bhaaskaran, "**Performance Analysis of Adder Architecture using Modified Pass transistor Adiabatic Logic Circuits**", IEEE International Conference on Smart Systems and Inventive Technology (ICSSIT), 2019, pp. 1003-1007. 9. Bhalerao, Abhishek L., Aishwarya Mane, Kartik Pensenwar, B. P. Bhuvana, A. Anita Angeline, and VS Kanchana Bhaaskaran, "**Design of energy efficient carry lookahead adder using novel CSIPGL adiabatic logic circuit.**" In Journal of Physics: Conference Series, vol. 1716, no. 1, p. 012033. IOP Publishing, 2020. 10. Ramkumar E, Gracin D, Rajkamal D, Bhuvana BP and V S Kanchana Bhaaskaran, "**Design and Analysis of Low Power and High Speed FinFET Based Hybrid Full Adder/Subtractor Circuit (FHAS)**" presented in 6th IEEE International Symposium on Smart Electronic Systems (iSES), 2020.
FDP & Workshop Attended Details:	1. Attended one day workshop on "**Digital VLSI Design using Industry standard EDA tools & Optimization Methodologies**" on March, 2014 in VIT University. 2. Participated in Faculty Development Programme on "**Research Paper Writing**" on February 2014 in Bharath University, Chennai. 3. Attended two days Research Programme on "**MATLAB Based Training on neural networks in Engineering Applications**" on February, 2013 in Kongu Engineering College. 4. Attended two days workshop on "**Hands on Training in LabVIEW**" on May, 2012 in Sona College of Technology in association with NI Systems Pvt Ltd. 5. Attended one day workshop on "**RF Technologies, Measurements and Applications**" on March,2012 conducted by Agilent Technologies in Sona College of Technology. 6. Participated in National Seminar on "**Indigenous Nanomaterials Development for Industrial Applications (INDIA)**" on February 2012 in Anna University, Chennai.

	7. Participated in two-day workshop on "**Digital system design using Cadence Tools**" on March 2016 in VIT University, Chennai. 8. Participated in one day National Seminar on "**5G and IoT – Intro, Development and Standards**" on Feb 2018 in VIT University, Chennai. 9. Participated in 3 days Online FDP on "**eSim**" organized by Vellore Institute of Technology (VIT) and Teaching learning Centre of IIT Bombay 14th May 2020 to 16th May 2020. 10. Participated in the Technical Webinar on "**Biomedical Applications of Fiber Bragg Grating Sensors**" on 18th May, 2020 organized by SRM Institute of Science and Technology, Kattankulathur. 11. Participated in Webinar Series organized by the department of Electronics and Communication Engineering of Sri Manakula Vinayagar Engineering College from 25th to 29th May 2020. 12. Participated in 5 day online FDP on "**Emerging Technologies in Robotics**" from 26th to 30th May 2020 in Malla Reddy Engineering College, Secunderabad, Telangana. 13. Participated in AICTE Training And Learning (ATAL) Academy Online FDP on "**Artificial Intelligence**" from 7th Dec 2020 to 11th Dec 2020 at Sri Sairam Engineering College. 14. Participated in the Faculty Development Program on "**Insight of Analog And Digital IC Design : Industry and Research Perspective (IADICD - 2020)**" during 14th - 19th December 2020 organized by Department of Electronics and Communication Engineering, SRM IST, Kattankulathur. 15. Participated in 3-days online FDP "**Effective strategies to improve Mentor – Mentee bonding**" organized by Easwari Engineering College, during 20th Jan 2021 to 22nd Jan 2021.
Professional Membership:	International Association of Engineers (IAENG)